Designing a High-Efficiency, 300-W, Wide Mains Interleaved PFC

Prepared by: Joel Turchi
ON Semiconductor

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

Overview

Application note AND8355 presents the main characteristics and merits of an interleaved PFC. This paper proposes the key steps to designing an interleaved PFC driven by two NCP1601. The process is practically illustrated on a 300−W, universal mains application:

- *Maximum output power: 300 W*
- *Input voltage range: from 90 V_{rms} to 265 V_{rms}*
- *Regulation output voltage: 390 V*
- *Clamp frequency: 120 kHz*

This solution lies on the Frequency Clamped Critical conduction mode (FCCrM) that limits the switching frequency spread and by this means, minimizes the switching losses. For an optimal efficiency over the whole power range, the solution also implements the frequency fold−back function to further reduce the light load losses by lowering the switching frequency. AND8356 reports the performance of this solution.

Introduction

One drawback of the Critical conduction Mode (CrM) circuits is that the switching frequency tends to become very high at light load (up to hundreds of kHz depending on the PFC design). These characteristics lead to high switching losses, possible noise issues and to the need for relatively big inductors to limit the switching frequency higher levels.

The NCP1601 is an 8−pin PFC controller designed to operate in Frequency Clamped Critical conduction (FCCrM). FCCrM clamps the switching frequency to overcome the above difficulty. It is worth noting that FCCrM does not simply clamp the switching frequency but in addition, it modulates the on−time to compensate the possible dead−times. As a matter of fact, it automatically transitions from the CrM and DCM (and vice versa) modes in a very clean manner: the input current keeps properly shaped and there is no discontinuity in the power transfer.

One NCP1601 per branch is implemented to drive each phase in FCCrM. As voltage mode controllers, the two circuits force the same MOSFET on−time in both branches as long as they share the same control voltage (to do so, the control pin of the two circuits are shorted). The demagnetization time that only depends on the conduction time and on the line and output voltages is then the same in both branches as well

$$\left(t_{demag} = t_{on} \cdot \frac{V_{in}}{V_{out} - V_{in}}\right).$$

Hence if we neglect the tolerance in the timing circuitry that for each circuit, adjusts the on−time in response to the control signal, the current cycle duration is the same in the two branches even if their respective coils do not have the same inductance.

Finally, the only source of current unbalancing is the inductor tolerance. One can easily show that the current sharing is governed by the following equation:

$$\frac{I_{in(branch1)}}{I_{in(branch2)}} = \frac{L_{branch2}}{L_{branch1}}$$

Where:

- $I_{in(branch1)}$ and $I_{in(branch2)}$ are the averaged input current drawn by phase 1 and phase 2 respectively
- $L_{branch1}$ and $L_{branch2}$ are the inductance values of phase 1 and phase 2 respectively

Practically, if the inductance tolerance is ±5%, the maximum deviation between the current of the branches is 10%.

NCP1601 Synchronization

The NCP1601 oscillator consists of an external capacitor, the voltage of which swings between the 3.5−V lower threshold and the 5−V upper one. The charge and discharge phases are controlled by internal current sources (about 50 μA are permanently sourced by the pin leading to a 50 μA charge current, 100 μA are sunk for the discharge phase only to obtain a 50−μA discharge current).

Each time, the capacitor voltage goes below 3.5 V and hence enters a new charge phase, the circuit sets the PWM latch that keeps set until a new drive turn high occurs.

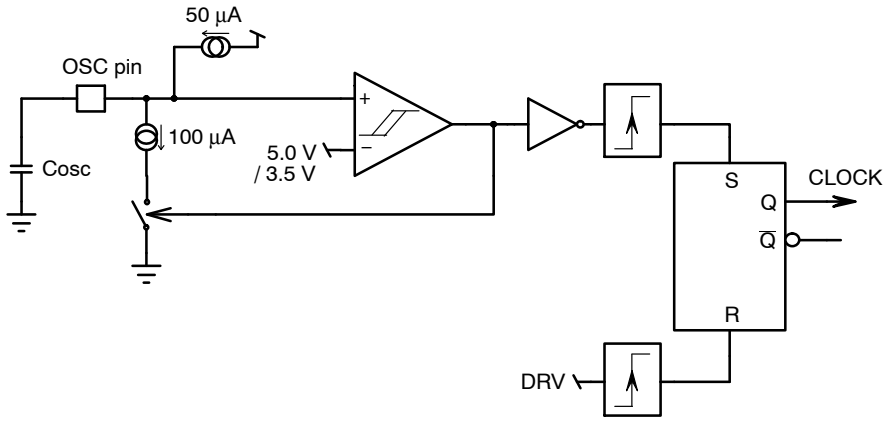

Figure 1. NCP1601 Clocks Generation

Hence, there are two cases:

- The PFC stage operates in fixed frequency. When the oscillator voltage goes below the 3.5−V low threshold, a clock is generated that immediately induces the next drive pulse. The switching frequency is the oscillator one (refer to Figure 2).
- The PFC stage operates in critical conduction mode. In this condition, the switching frequency is lower than the oscillator one. When the oscillator voltage goes below 3.5 V, a clock is generated but the driver cannot turn high until the core is reset (refer to Figure 3).

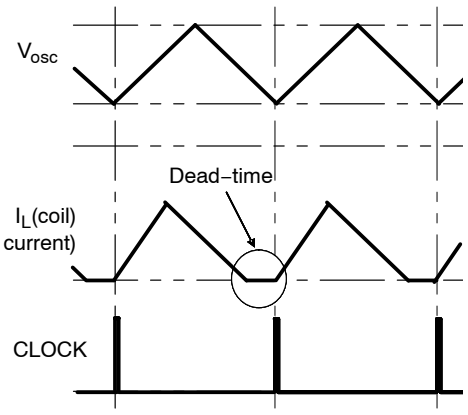

Figure 2. Generation of the Clock Signals – Fixed Frequency

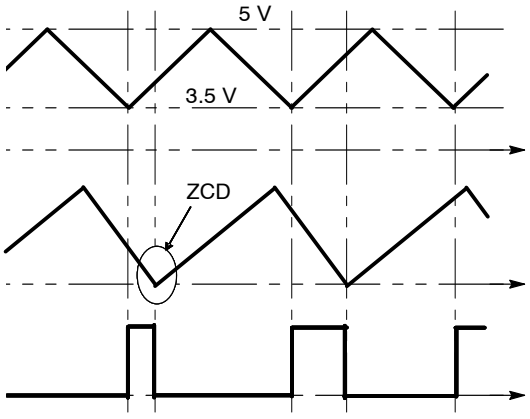

Figure 3. Generation of the Clock Signals – Critical Conduction Mode

Synchronization of the Two Stages in the Interleaved Application

As portrayed by Figure 4, the two NCP1601 circuits are synchronized to the "DRV2" signal (driver of phase 2). One could have chosen "DRV1" as the triggering signal but in this case, the C_t circuitry for which the two branches are not fully symmetrical, should have to be also reversed.

When "DRV2" turns high, the (C_{20}, R_{31}) network generates a positive voltage pulse across R_{31}. The D_{14} ZENER diode clamps this pulse and guarantees the full C_{20} discharge when DRV2 is in low state. If C_{20} is large enough to properly bias the ZENER diode (*), a (0 V, 6.8 V) calibrated pulse is obtained across D_{14}. This signal is applied to the oscillator pin of the two controllers through a diode.

The oscillator capacitors (C_{14} for circuit of branch 1, C_{15} for circuit of branch 2) are then charged to about 6 V. As this voltage exceeds the upper oscillator threshold (5 V), the two circuits enter the discharge phase.

Capacitors C_{14} and C_{15} are discharged by the internal current source (about 50 μA) and the external resistors R_{26} and R_{27} respectively. Resistors R_{28} and R_{29} can also speed−up the discharge or at the contrary slow it down according to the V_{FR} voltage. V_{FR} is the voltage that controls the frequency fold−back at light load. As explained in the "frequency fold−back" section, this voltage is near zero at full load (and hence tends to shorten the discharge phase) and is increased at light load (to extend the discharge phase and hence reduce the switching frequency).

* Like proposed here, use "DRV2" that is the driver pin signal, rather than the gate signal which dV/dt may be much lower due the MOSFET capacitances. With the connection to the drive pin, C_{20} = 2.2 nF should give good results.

Once a pulse has occurred across the D_{14} ZENER diode, the next clock for branch 1 is generated when the signal SYNC1 (voltage across C_{14}) drops below 3.5 V that is, after a delay τ that meets the following equation:

$$V_{oscL} = \left(V_{oscH} - \left(R_{osc1} \cdot \frac{V_{FR}}{R_{28}}\right) + (R_{osc1} \cdot I_{DISCH})\right) \cdot e^{\frac{-\tau}{R_{osc1} \cdot C_{osc1}}} + \left(R_{osc1} \cdot \frac{V_{FR}}{R_{28}}\right) - (R_{osc1} \cdot I_{DISCH})$$

Where,

- V_{oscH} represents the level at which the oscillator pin is charged by the DRV2 pulse
- V_{oscL} represents the oscillator low threshold (3.5 V)
- R_{osc1} is R_{26} // R_{28}
- I_{DISCH} is the NCP1601 internal discharge current (50 μA)
- C_{osc1} is the oscillator capacitor for the NCP1601 of branch 1

Hence:

$$\tau = -R_{osc1} \cdot C_{osc1} \cdot \ln\left(\frac{V_{oscL} - \left(R_{osc1} \cdot \frac{V_{FR}}{R_{28}}\right) + (R_{osc1} \cdot I_{DISCH})}{V_{oscH} - \left(R_{osc1} \cdot \frac{V_{FR}}{R_{28}}\right) + (R_{osc1} \cdot I_{DISCH})}\right)$$

Replacing R_{osc1}, V_{oscL}, V_{oscH}, R_{28} and I_{DISCH} by their value, it comes:

$$\tau \cong 23500 \cdot C_{osc1} \cdot \left(0.43 - \ln\left(\frac{1 - \frac{V_{FR}}{16.3}}{1 - \frac{V_{FR}}{25.0}}\right)\right)$$

Finally:

- At full load, V_{FR} is nearly zero and: $\tau_{(full\_load)} \cong 10100 \cdot C_{osc1}$
- At light load, V_{FR} is nearly V_{CC} that is 15 V and: $\tau_{(light\_load)} \cong 48000 \cdot C_{osc1}$

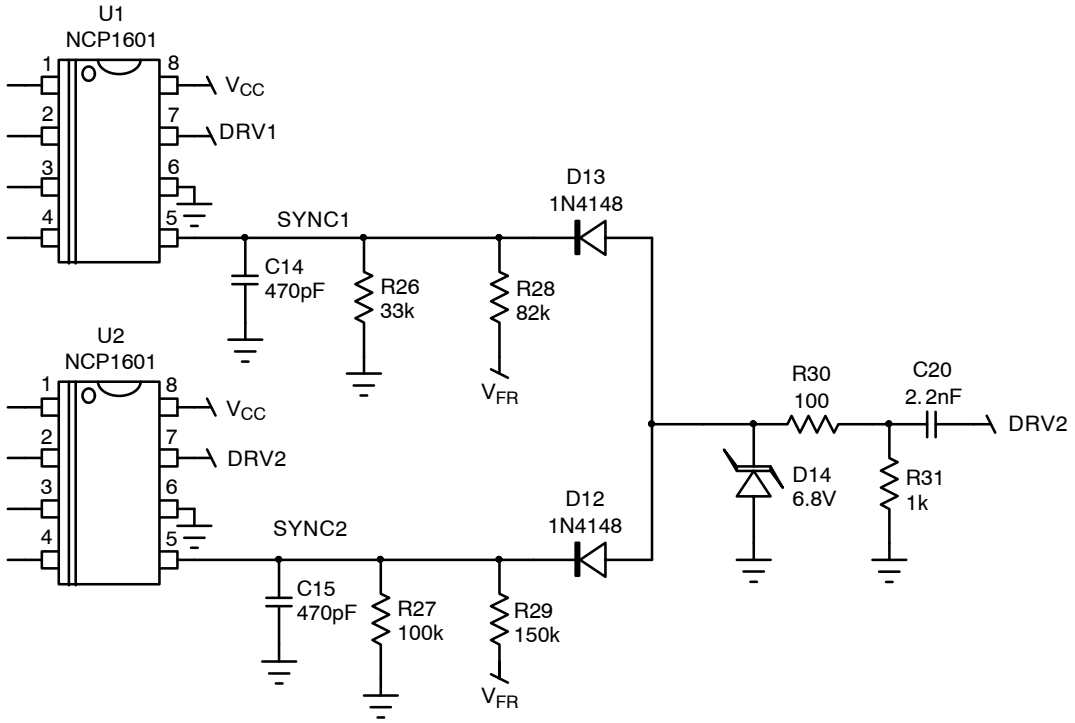

Figure 4. Synchronization Circuitry

Similarly, one can compute the delay τ_2 between the DRV2 turn on and the next clock for branch 2. This delay must meet the following equation:

$$V_{oscL} = \left(V_{oscH} - \left(R_{osc2} \cdot \frac{V_{FR}}{R_{28}}\right) + (R_{osc2} \cdot I_{DISCH})\right) \cdot e^{\frac{-\tau}{R_{osc2} \cdot C_{osc2}}} + \left(R_{osc2} \cdot \frac{V_{FR}}{R_{28}}\right) - (R_{osc2} \cdot I_{DISCH})$$

Where,

- R_{osc2} is R_{27} // R_{29} (60 kΩ)
- C_{osc2} is the oscillator capacitor for the branch 2 NCP1601

Hence:

$$\tau_2 = -R_{osc2} \cdot C_{osc2} \cdot \ln\left[\frac{V_{oscL} - \left(R_{osc2} \cdot \frac{V_{FR}}{R_{29}}\right) + (R_{osc2} \cdot I_{DISCH})}{V_{oscH} - \left(R_{osc2} \cdot \frac{V_{FR}}{R_{29}}\right) + (R_{osc2} \cdot I_{DISCH})}\right]$$

Replacing R_{osc1}, V_{oscL}, V_{oscH}, R_{28} and I_{DISCH} by their value, it comes:

$$\tau_2 \cong 60000 \cdot C_{osc2} \cdot \left[0.325 - \ln\left[\frac{1 - \frac{V_{FR}}{16.25}}{1 - \frac{V_{FR}}{22.50}}\right]\right]$$

Finally:

At full load, V_{FR} is nearly zero and:

$$\tau_{2(full\_load)} \cong 19500 \cdot C_{osc2} \cong 1.93 \cdot \tau_{(full\_load)}$$

At light load, V_{FR} is nearly V_{CC} that is 15 V and:

$$\tau_{2(light\_load)} \cong 109750 \cdot C_{osc2} \cong 2.28 \cdot \tau_{(light\_load)}$$

We can note that if (C_{osc1} = C_{osc2}), the chosen resistors enable to keep τ_2 in the range of (2.τ) even when the frequency reduces (frequency fold−back), as required to obtain an out−of−phase operation.

In our case, we select (C_{osc1} = C_{osc2} = 470 pF) to obtain:

At full load,

$$\tau_2 \cong 19500 \cdot 470 \cdot 10^{-12} \cong 9.16\ \mu s$$

which leads to 110 kHz per branch

At light load,

$$\tau_2 \cong 109750 \cdot 470 \cdot 10^{-12} \cong 51.58\ \mu s$$

This means that the minimum frequency that can be obtained is 20 kHz per branch with V_{CC} = 15 V.

The two following figures illustrate the above analysis.

Figure 5 is obtained in a moderate load condition. The system operates in fixed frequency. The frequency is in the range of 50 kHz per branch. As wished for out−of−phase operation, ($\tau_2 \cong 2 \cdot \tau$).

Figure 6 is obtained at heavy load. The system operates in critical conduction mode. The frequency is in the range of 110 kHz per branch. Again an out−of−phase operation is obtained with the help of the “phase shift compensation circuitry” (See “maintaining a 180° Phase Shift” section).

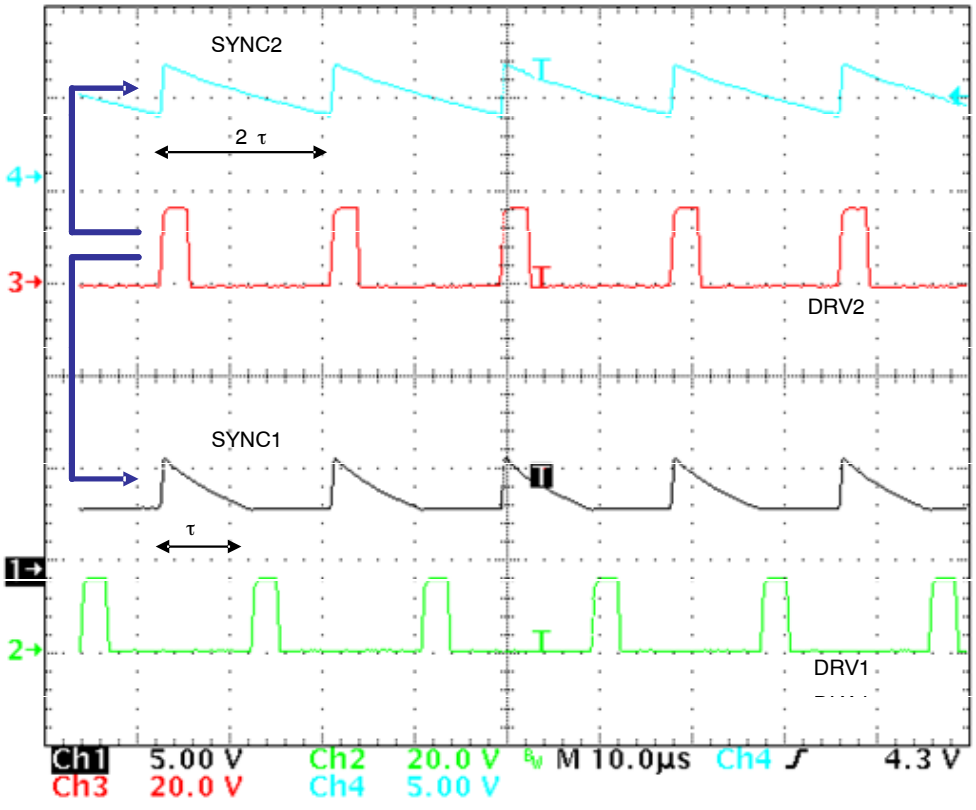

Figure 5. Synchronization in Fixed Frequency Operation

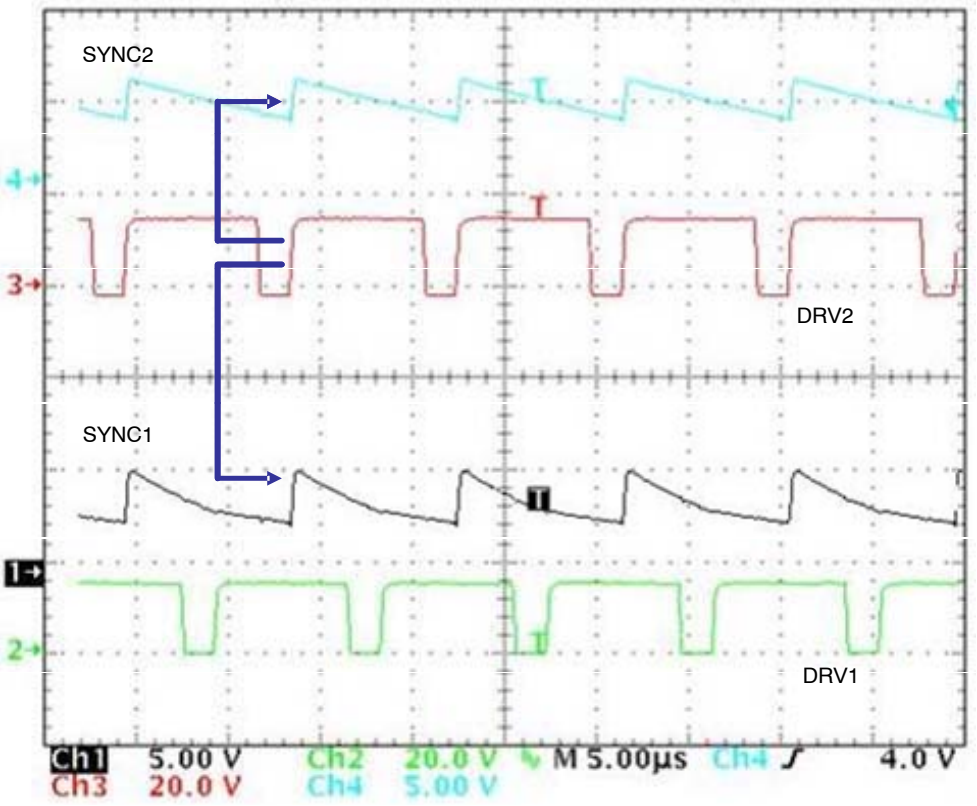

Figure 6. Synchronization in Critical Conduction Mode Operation

Frequency Fold−back

A very simple circuitry is implemented that lowers the switching frequency when the duty−cycle reduces. A npn transistor is operated to be on when any of the two drives is high.

In low line, full load when there is always one of the two drives in high state, the npn transistor is permanently on and its collector voltage is low. On the contrary, the duty−cycle reduces in light load and there are large parts of the interleaved PFC switching periods when the two drives are low. During these intervals of time, the npn transistor is off and its collector rises to V_{CC}. These V_{CC} pulses are integrated to form a dc voltage (V_{FR}) representative of the MOSFETs loading:

- V_{FR} is high when the system is in light load and/or at high line
- V_{FR} is low when the system is in heavy load, low line.

The voltage is applied to the oscillator pin of the two NCP1601. The injection is performed through resistor R_{28} for branch 1 and R_{29} for branch 2. These resistors have values (82 kΩ and 150 kΩ, respectively) that enable to maintain the out−of−phase operation in light load (see the “synchronization of the two stages in the interleaved application” section).

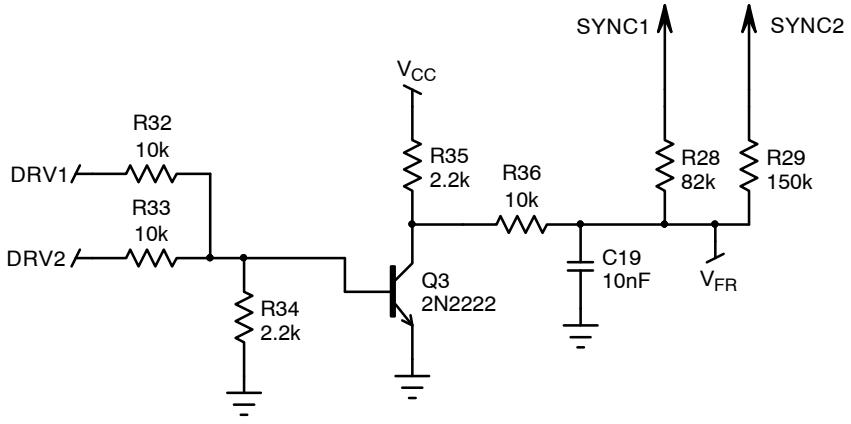

Figure 7. Circuitry for Frequency Fold−back

Dimensioning the Power Components

Basically, Two 150−W FCCrM PFC stages are to be designed. This chapter will not detail the dimensioning of the power components in very deep details since their computation is traditional. However, the main selection criteria and equations are reminded.

Inductor Selection

In CrM and in FCCrM (assuming CrM operation at low line, full load), the (maximum) peak and rms inductor currents within one branch are:

$$(I_{L(pk)})_{MAX} = \frac{2\sqrt{2} \cdot \left(\frac{P_{out(max)}}{2}\right)}{\eta \cdot (V_{in(rms)})_{LL}} = \frac{2\sqrt{2} \cdot 150}{0.92 \cdot 90} \cong 5.1\ A$$

And:

$$(I_{L(rms)})_{MAX} = \frac{(I_{L(pk)})_{MAX}}{\sqrt{6}} \cong \frac{5.1}{\sqrt{6}} = 2.1\ A$$

Where:

- $P_{out(max)}$ is the maximum level of the total output power (300 W)
- $(V_{in(rms)})_{LL}$ is the lowest line rms input voltage (90 V)
- η is the PFC stage efficiency (assumed to be 92% to have some margin)

As aforementioned, the frequency clamp for the two branches is set to about 110 kHz. The inductor must be large enough so that Critical conduction Mode is obtained at low line, full load where the conditions are the most severe.

This constraint leads to the equation below (where $f_{sw(max)}$ is the 110−kHz clamp frequency):

$$L \geq \frac{\eta \cdot (V_{in(rms)})_{LL}{}^2 \cdot \left(\frac{V_{out}}{\sqrt{2}} - (V_{in(rms)})_{LL}\right)}{\sqrt{2} \cdot V_{out} \cdot \left(\frac{P_{out(max)}}{2}\right) \cdot f_{sw(max)}} = \frac{0.92 \cdot 90^2 \cdot \left(\frac{390}{\sqrt{2}} - 90\right)}{\sqrt{2} \cdot 390 \cdot 150 \cdot 110\ k} \cong 150\ \mu H$$

Finally, a 150 μH / 6 A_{pk} / 2.5 A_{rms} coil was selected.

Power Semiconductors

The bridge diode should be selected based on the peak current rating and the power dissipation given by:

$$P_{bridge} = \frac{4\sqrt{2}}{\pi}\frac{V_f}{(V_{in(rms)})_{LL}}\frac{P_{out(max)}}{\eta} \cong 1.8\frac{V_f}{90}\frac{300}{0.92} \cong 6.5\ V_f$$

Assuming a 1−V forward voltage per diode (V_f = 1 V), the bridge approximately dissipates 6.5 W.

For each branch, the MOSFET is selected based on the peak voltage stress ($V_{out(max)}$ + margin) and on the rms current flowing through it ($I_{M(rms)}$):

$$I_{M(rms)} = \frac{2 \cdot \left(\frac{P_{out(max)}}{2}\right)}{\sqrt{3} \cdot \eta \cdot (V_{in(rms)})_{LL}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot (V_{in(rms)})_{LL}}{3 \cdot \pi \cdot V_{out}}} = \frac{2 \cdot 150}{\sqrt{3} \cdot 0.92 \cdot 90}\sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot 90}{3 \cdot \pi \cdot 385}} \cong 1.8\ A$$

Using a 600−V, 0.4−Ω FET (SPP11N60), will give conduction losses of (assuming that $R_{DS(on)}$ increases by 80% due to temperature effects):

$$P_{cond} = I_{M(rms)}{}^2 \cdot R_{DS(on)} = 1.8^2 \cdot 0.4 \cdot 1.8 \cong 2.3\ W$$

This computation is valid for one branch. As there are two phases to consider, the total MOSFETs conduction losses are actually twice (4.6 W).

Switching losses are extremely hard to predict. They are not computed here. As a rule of the thumb, it is considered that the switching losses are in the same range as the conduction ones.

The input bridge that rectifies the line voltage and the MOSFETs of the two branches share the same heat−sink. Based on above computations, the total power to be dissipated is in the range of: (6.5 + 4.6 + 4.6 ≅ 16 W). A 2.9−°C/W heat−sink (ref. 437479 from AAVID THERMALLOY) is implemented. It limits the rise of the case temperature (of the input bridge and MOSFETs applied to it) to about 50° compared to the ambient temperature.

Interleaved PFC requires two boost diodes (one per branch). No reverse recovery issues to worry about. Simply, they must meet the correct voltage rating ($V_{out(max)}$ + margin) and exhibit a low forward voltage drop. Supposing a perfect current sharing, the average diode current is the half of the load one

$$\left(I_{D1(avg)} = I_{D2(avg)} = \frac{I_{D(tot)_{avg}}}{2} = \frac{I_{LOAD}}{2} = \frac{P_{out}}{2 \cdot V_{out}} \cong 0.39\ A\right)$$

So, the losses are about ($I_{LOAD} \cdot V_f$ / 2) per diode, i.e., less than 500 mW per diode using MUR550 rectifiers. For each phase, the peak current seen by the diode will be the same as the corresponding inductor peak current.

Two axial MUR550 are selected.

Bulk Capacitor Design

The output capacitor is generally designed considering 3 factors:

1. The maximum permissible low frequency ripple of the output voltage. The input current and voltage being both sinusoidal, PFC stages deliver a squared sinusoidal power that matches the load power demand in average only. As a consequence, the output voltage exhibits a low frequency ripple (e.g., 100 Hz ripple in Europe or 120 Hz in USA) that is inherent to the PFC function
2. The rms magnitude of the current flowing through the bulk capacitor. Based on this computation, one must estimate the maximal permissible ESR not to cause an excessive heating.
3. The hold−up time. It can be specified that the power supply must provide the full power for a short mains interruption that is the so called hold−up time. The hold−up time is generally in the range of 10 or 20 ms.

The output voltage ripple is given by:

$$\Delta V_{out(p-p)} = \frac{P_{out}}{2\pi \cdot f_{line} \cdot C_{out} \cdot V_{out}}$$

The capacitor rms current is given by (assuming a resistive load):

$$I_{C(rms)} = \sqrt{\frac{16 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot (V_{in(rms)})_{LL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out}}\right)^2}$$

Finally the following equation expresses the hold−up time:

$$t_{hold-up} = \frac{C_{out} \cdot (V_{out}^2 - V_{out(min)}^2}{2 \cdot P_{out}}$$

Where $V_{out(min)}$ is the minimal bulk voltage necessary to the downstream converter to keep properly feeding the load.

The hold−time being not considered here, a 100−μF capacitor was chosen to satisfy the other above conditions. The peak−peak ripple is 25 V (±3% of V_{out}) and the rms current is 1.4 A.

Regulation Circuitry

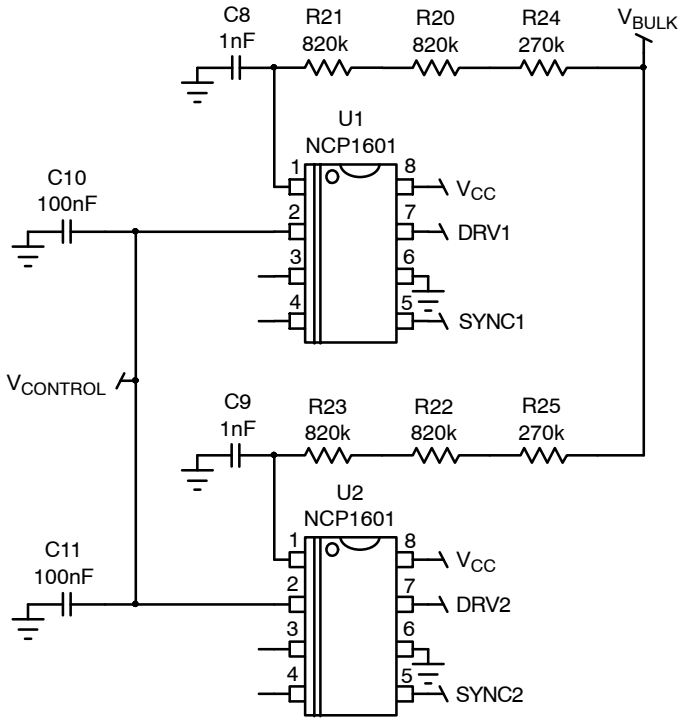

Figure 8. Regulation Circuitry

The two NCP1601 must force the same MOSFET on−time. To do so, the two IC's must have the same control voltage. Practically, pin2 of the NCP1601 that controls the first phase is connected to pin2 of the NCP1601 that drives the second phase. For each device, a 100−nF compensation capacitor should be placed between pin2 and ground. Short connections are recommended to optimize the noise immunity.

A global 200−nF capacitor is generally enough. Type−2 compensation can be implemented for better dynamic performance if necessary.

The NCP1601 is designed to receive a feedback current that is compared to a 200−μA reference current. For each NCP1601, two or more (for safety reasons) resistors are to be connected between the output voltage rail and the feedback pin (pin1). The resistance must be selected so that

pin1 absorbs 200 μA when the output voltage is at the desired level:

$$R_{FB} = \frac{V_{out(nom)} - V_{pin1}}{200 \cdot 10^{-6}}$$

Where:

- $V_{out(nom)}$ is the desired output voltage
- V_{pin1} is the pin1 voltage (about 3 V)

In our case:

$$R_{FB} = \frac{390 - 3}{200 \cdot 10^{-6}} = 1.935\ M\Omega$$

In our application, we choose three resistors in series (820 kΩ + 820 kΩ + 270 kΩ) for a global 1910 kΩ resistance. For each circuit, it is recommended to add a 1−nF capacitor between pin1 and ground to filter the possible surrounding noise.

C_t Capacitor

For each controller, the capacitor that is applied to pin3 adjusts the maximum on−time and hence, the maximal power that the branch can deliver.

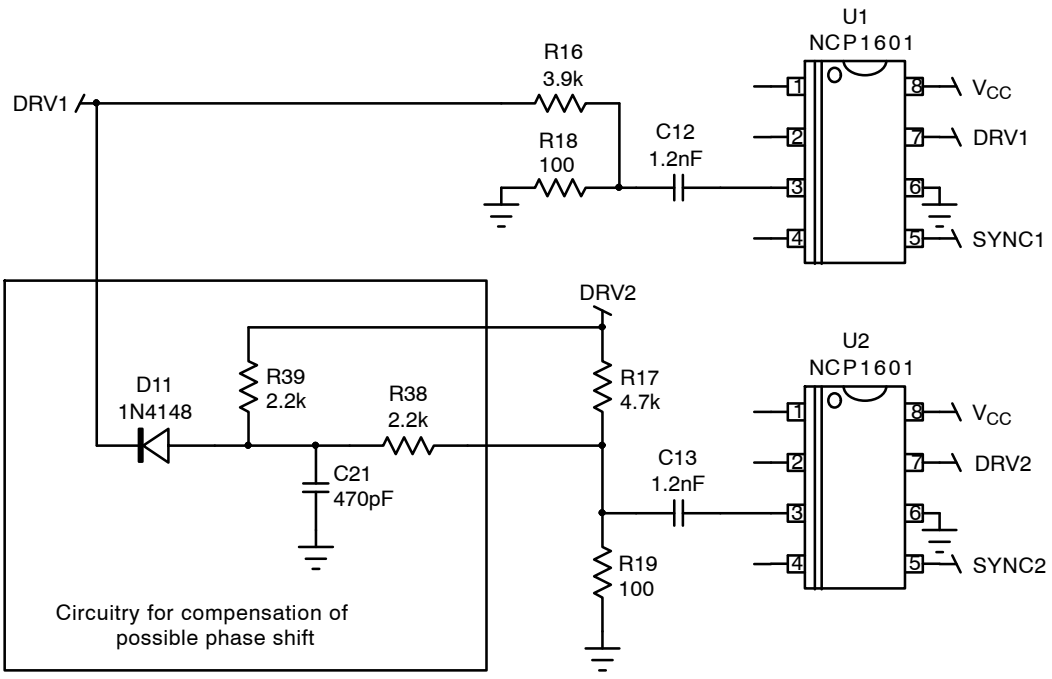

Figure 9. Timing Capacitor Circuitry

In the application, it can be noted that a portion of the drive signal offsets the pin 3 voltage. This offset is to reduce the minimum on−time at light load and to help maintain the 180° phase shift. To the light of Figure 9, we can note that:

- Branch 1 has a larger offset than branch 2:
  - The phase 1 offset is:

$$\left(\frac{R_{18}}{R_{18} + R_{16}} \cdot V_{CC} = \frac{100}{3900 + 100} \cdot V_{CC}\right)$$

that is, 375.0 mV with V_{CC} = 15 V.

The phase 2 offset is:

$$\left(\frac{R_{19}}{R_{19} + R_{17}} \cdot V_{CC} = \frac{100}{4700 + 100} \cdot V_{CC}\right)$$

that is, 312.5 mV with V_{CC} = 15 V.

- Branch 2 has another source of offset that is provided by the “circuitry for compensation of possible phase shift”.

The small imbalance in the offsets is explained in the “Maintaining a 180° Phase Shift” section.

Let’s assume that the resistors that are used for the offset can be re−used in any design, the C_t capacitor must now be computed as a function of the power to be delivered.

To do so, the maximum available on−time should be computed for branch 1 that has the larger offset. As the normal pin3 swing is 1 V and since the pin3 charge current is 100 μA:

$$t_{on(max)} = C_{pin3} \cdot \frac{1\ V - 375\ mV}{100 \cdot 10^{-6}} = 6250 \cdot C_{pin3}$$

In our application, we need to provide about 160 W (input) per branch. The following equation gives the maximum power that can be delivered as a function of the maximum on−time (CrM operation):

$$(P_{in(avg)})_{MAX} = \frac{(V_{in(rms)})_{LL}^{2}}{2 \cdot L} \cdot t_{on(max)}$$

From the above equations, we can deduce:

$$C_{pin3} = \frac{2 \cdot L \cdot (P_{in(avg)})_{MAX}}{6250 \cdot (V_{in(rms)})_{LL}^{2}}$$

In our application:

$$C_{pin3} = \frac{2 \cdot 150 \cdot 10^{-6} \cdot 160}{6250 \cdot 90^2} \cong 948\ pF$$

1−nF is the closed standard capacitor. However, for a 20% necessary margin, a 1.2−nF capacitor is selected and implemented in the two branches.

Maintaining a 180° Phase Shift

The synchronization circuitry tends to force a delay between the two branches. The phase shift is perfectly correct in fixed frequency mode but the operation can be altered when the circuit operates in critical conduction mode. For instance, some distortion can result from a protection triggering that would turn off the MOSFETs of the two branches simultaneously. Also, perturbations like discrepancies in the actual on−time, can lead to a loss of the 180° phase shift and even to an in−phase operation that is also a stable operation point!

That is why, the synchronization is not sufficient by itself.

The difficulty is overcome by controlling the maximum overlap, that is, the maximum time for each the two drivers must be on simultaneously. More specifically, the drive that synchronizes the system (DRV2 in our application) is truncated when the overlap duration is excessive.

We can estimate the maximum overlap time by calculating the on−time and demagnetization time at low line, full load (top of the sinusoid).

For any of the two branches, the MOSFET conduction time and the demagnetization duration can be expressed as follows:

$$t_{on} = \frac{L \cdot I_{L(pk)}}{V_{in}}$$

$$t_{demag} = \frac{L \cdot I_{L(pk)}}{V_{out} - V_{in}}$$

Hence, if we ignore the short dead−time due the valley switching, the duration of a current cycle (that is the switching period) is:

$$t_{sw} = t_{on} + t_{demag} = \frac{L \cdot I_{L(pk)} \cdot V_{out}}{V_{in} \cdot (V_{out} - V_{in})}$$

The maximum overlap is the difference between the on−time of one driver and half the period when the other driver is supposed to turn high (out−of−phase operation). Hence:

$$t_{overlap(max)} = t_{on} - \frac{t_{sw}}{2} = \frac{L \cdot I_{L(pk)}}{V_{in}} \left(1 - \frac{V_{out}}{2 \cdot (V_{out} - V_{in})}\right)$$

In our application,

$$t_{overlap(max)} = \frac{150\ \mu \cdot 5.1}{125} \left(\frac{390 - 250}{2 \cdot (390 - 125)}\right) \cong 1.6\ \mu s$$

The circuit for compensation of possible phase shift, charges the capacitor C_{21} of Figure 9 when the two drives are on and the obtained ramp is added to the timing ramp of DRV2, resulting on the following additional offset on the (phase 2) C_t pin:

$$offset \cong \frac{100}{R_{38} + R_{39}} \cdot V_{CC} \cdot \left(1 - e^{\frac{t}{R_{38} \| R_{39} \cdot C_{21}}}\right)$$

From the above equation, we can deduce the capacitor that exactly compensates the difference in the phase 1 and phase 2 C_t pin offset (62.5 mV) at the end of the 1.6 μs:

$$C_{21} = \frac{-1.6\ \mu s}{(R_{38} \| R_{39}) \cdot \ln\left(1 - \frac{62.5\ mV \cdot (R_{38} + R_{39})}{R_{19} \cdot V_{CC}}\right)} \cong 7.2\ nF$$

In practice, it appears that a 470−pF capacitor that leads to a more abrupt reaction to overlaps, is also a good (conservative) choice. A 470−pF capacitor is then implemented.

V_{CC} and Drivers

The V_{CC} voltage biases the two controllers but also the frequency fold−back circuitry. The V_{CC} level slightly influences:

- The voltage available to drive the MOSFET gate (as in any PFC stage)
- The frequency fold−back circuitry
- The C_t pin offsets

The V_{CC} voltage must remain below 18 V.

The design is optimized for (V_{CC} = 15 V). The V_{CC} voltage should be set preferably in this range. A lower V_{CC} voltage would mainly result in a smaller reduction of the switching frequency in light load (refer to the frequency fold−back section).

As there are two circuits to feed, it is recommended to locally decouple the V_{CC} pin of each of them. This is the role of the C_{19} and C_{20} ceramic capacitors of Figure 13.

In any CrM or FCCrM PFC stage, the MOSFET can be turned on in a relatively slow manner because there is no current stress. On the other hand, the opening must be fast to limit the switching losses. As shown in the application schematic of Figure 13, pnp transistors ("Q_1" for phase 1 and "Q_2" for phase 2) speed−up the turn off of the MOSFETs.

Current Sensing

Figure 10 portrays the NCP1601 current sensing method.

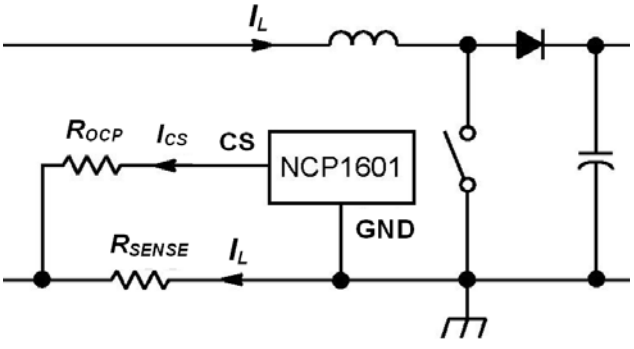

Figure 10. Negative Sensing

A current sense resistor R_{SENSE} is placed in the return path so that the coil current that flows through it generates a negative voltage. A resistor R_{OCP} is inserted between the

R_{SENSE} negative terminal and the CS pin (current sense pin – pin 4). The NCP1601 is designed to maintain 0 V on the CS pin. To do so, pin4 sources the current I_{CS} that together with the external resistor R_{OCP} forms an offset voltage that cancels the R_{SENSE} negative voltage.

More specifically:

$$-(R_{SENSE} \cdot I_L) + (R_{OCP} \cdot I_{CS}) = 0$$

The precedent equation leads to:

$$I_{CS} = \frac{R_{SENSE}}{R_{OCP}} \cdot I_L$$

Hence, pin4 sources the I_{CS} signal that is proportional to the inductor current. When I_{CS} exceeds the 200−μA internal reference, the circuit detects an over−current and disables the drive. The over−current can then be programmed using two elements R_{OCP} and R_{SENSE}.

We select R_{SENSE} to obtain an optimal compromise between noise immunity and losses. A good choice is generally the value that leads to about 0.25% efficiency losses in it:

$$R_{SENSE} \cdot I_{in(rms)}^{\ 2} = 0.25\% \cdot P_{in(avg)}$$

If one neglects the high frequency ripple of the input current, one can deduce the following R_{SENSE} expression:

$$R_{SENSE} = 0.25\% \cdot \frac{P_{in(avg)}}{I_{in(rms)}^{\ 2}} = 0.25\% \cdot \frac{V_{in(rms)}^{\ 2}}{P_{in(avg)}}$$

In our case,

$$R_{SENSE} = 0.25\% \cdot \frac{90^2}{320} \cong 63\ m\Omega$$

In practice, (R_{SENSE} = 75 mΩ) is chosen. We have now to select R_{OCP} to set the proper current limit.

Permissible Current – R_{OCP} Selection

Our interleaved circuit monitors the total current. From the formulae given in AND8355, we can deduce that the maximum total current is:

$$(I_{L(tot)})_{MAX} = 2\sqrt{2} \cdot \frac{P_{in(avg)}}{(V_{in(rms)})_{LL}} \cdot \left[1 - \frac{V_{out}}{4 \cdot \left(V_{out} - \left(\sqrt{2} \cdot (V_{in(rms)})_{LL}\right)\right)}\right] \quad \text{if } (V_{in(rms)})_{LL} \le \frac{V_{out}}{2\sqrt{2}}$$

$$(I_{L(tot)})_{MAX} = 2\sqrt{2} \cdot \frac{P_{in(avg)}}{(V_{in(rms)})_{LL}} \cdot \left(1 - \frac{V_{out}}{4\sqrt{2} \cdot (V_{in(rms)})_{LL}}\right) \quad \text{if } (V_{in(rms)})_{LL} \le \frac{V_{out}}{2\sqrt{2}}$$

In our case,

$$V_{in(rms)LL} = 90 \le \frac{V_{out}}{2\sqrt{2}} = \frac{385}{2\sqrt{2}} \cong 136.$$

Hence,

$$(I_{L(tot)})_{MAX} = 2\sqrt{2} \cdot \frac{326}{90} \cdot \left(1 - \frac{390}{4 \cdot \left(390 - (\sqrt{2} \cdot 90)\right)}\right) \cong 6.4\ A$$

In practice, the OCP protection should not trigger during "normal" transients. Hence, it is recommended to place the limit about 50% higher, that is 10 A in our case.

$$R_{OCP} = \frac{R_{SENSE} \cdot (I_{L(tot)})_{MAX}}{I_{OCP}} = \frac{75\ m \cdot 10}{200\ \mu} = 3.75\ k\Omega$$

In practice, one (R_{ocp} = 3.9 kΩ) resistor is chosen for each branch.

Important Remark:

It is recommended to clamp the R_{SENSE} negative voltage to prevent excessive levels during the start−up and possible overload sequences (when huge in−rush currents can take place). Otherwise, the circuit may not be able to properly control the MOSFET during such stressing transients. In the application schematic, a 1N5406 (D_{12}) plays the role of the protecting diode. Actually, this diode does not need to be a high voltage one. It only must be able to sustain the in−rush current and its forward voltage must high enough so that the R_{SENSE} voltage is not clamped until the current largely exceeds its permissible level in normal operation. Otherwise, the clamping diode would prevent the R_{SENSE} voltage from being high enough to trigger the over−current protection.

Zero Current Detection

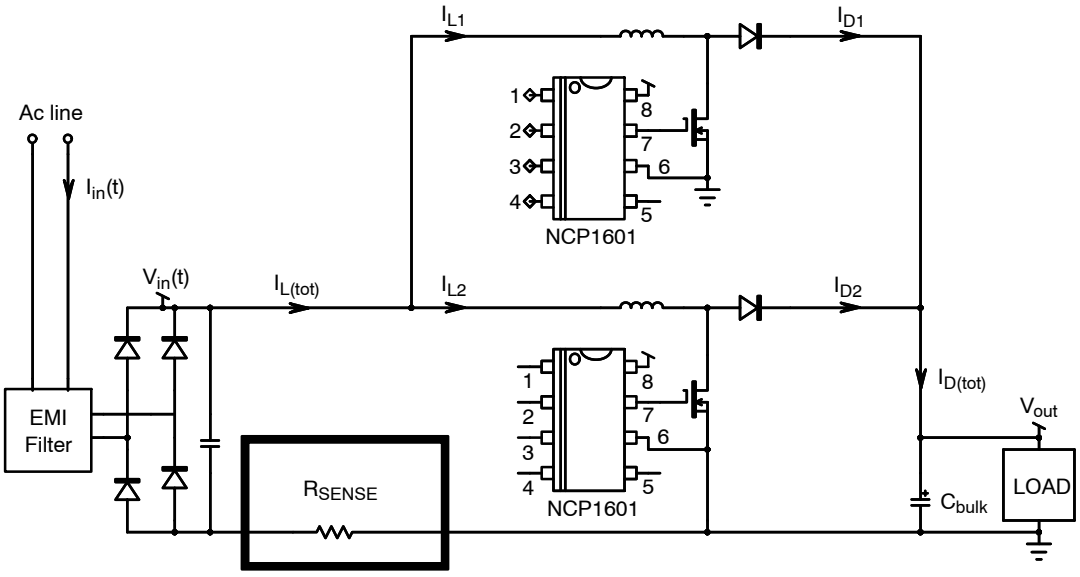

Figure 11. The Total Current is Sensed

The NCP1601 is designed to detect the core reset completion by directly sensing the current. Practically, in a conventional 1−phase PFC stage, the circuit monitors the coil current and when it is nearly zero, a ZCD signal is internally generated.

This solution is not valid anymore for an interleaved PFC stage. This is because the current sense resistor that is placed in the current return path, sees the total current absorbed by the two branches (see Figure 11). Hence, the voltage across R_{SENSE} is not representative of the current of any specific phase but of the total one. Therefore, this voltage cannot detect the core reset of a branch.

However, the R_{SENSE} voltage is utilized as portrayed by Figure 12.

To explain how it works, we have to consider the two following cases:

1. There is no current across R_{SENSE}. That simply means that there is no current flowing through both the two branches. No negative voltage being applied to its current sense pin, each NCP1601 naturally detects the core reset and can turn on the MOSFET of the branch it drives as soon as allowed by the synchronization signal.
2. A negative voltage biases the NCP1601 current sense pin as it occurs when one at least of the two branches conveys some current. However, since both circuits are identically biased, both phases are prevented from initiating a new cycle. A circuitry is then added to cancel the R_{SENSE} biasing of the current sense pin when the core reset occurs. As portrayed by Figure 12, this circuit operates as follows:
   - An auxiliary winding is coupled to the PFC inductor to provide a positive voltage when the MOSFET is on.
   - The network (C_6, R_2) generates a positive pulse whenever the auxiliary voltage rises up and in particular, at the end of a demagnetization phase. This positive pulse is clamped (and calibrated) by a 5−V ZENER diode (D_7).
   - A diode D_5 is to eliminate the negative pulses that take place across R_2 (when the circuit enters the demagnetization phase for instance) and that may influence the over−current protection. Another 1 kΩ (R_6) reduces the impedance at the cathode of the diode and ensures a proper biasing of D_5.
   - The voltage obtained across R_6 is then applied to the current sense pin to turn it positive. The R_{4x} resistor limits the current injected to pin4.

How to dimension these elements in a general manner?

1. D_5, D_7, R_2, R_{4x} and R_6 could keep the same value in any applications
2. C_6 is to be adapted to the dV/dt across the auxiliary winding. This dV/dt depends on the transition speed, on the input and output voltages and on the turn ratio. The turn ratio (N_{aux} / N_{prim}) is generally in the range of 0.1. C_6 must be high enough so that the D_7 ZENER diode trips when the core reset occurs.

This circuitry is to be applied to the two phases.

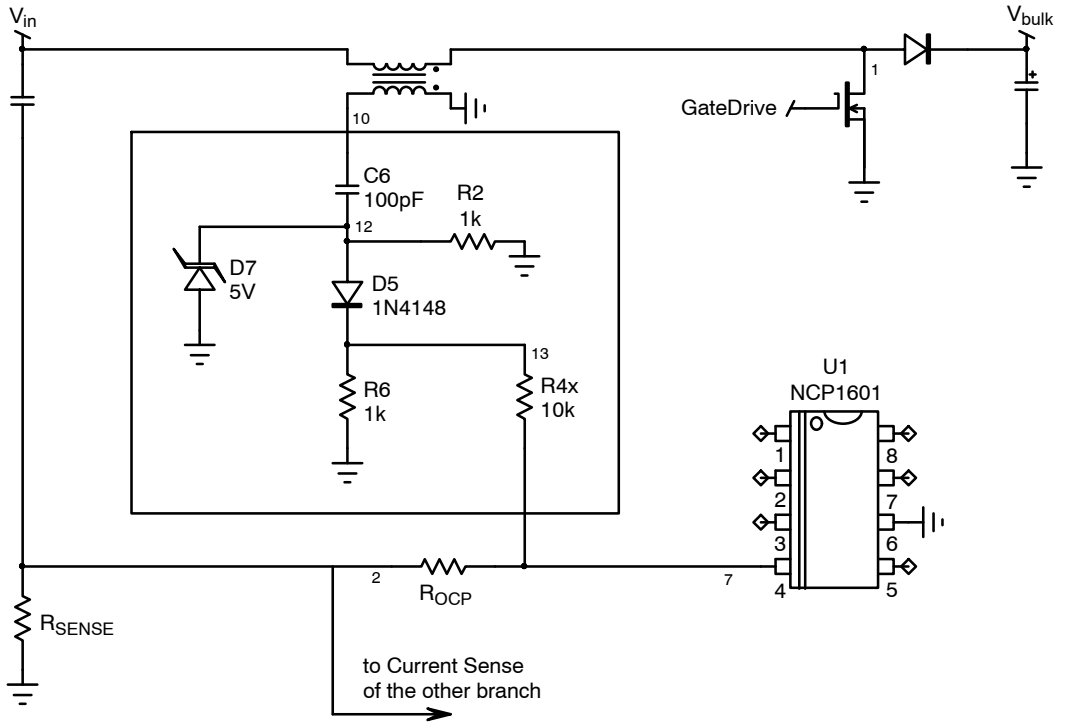

Figure 12. Demagnetization Circuit (one per branch is required)

Conclusions

This application note proposes the key equations and design criteria to build an efficient 2−NCP1601 interleaved PFC stage. The practical implementation of a 300−W, wide mains application illustrates the process. As the proposed approach is systematic and as a large part of the design can be "copied−pasted", the 2−NCP1601 solution can be easily applied to other applications.

For information on the performance of a 300−W interleaved PFC designed according to the proposed method, you can refer to AND8356. This application note shows that the efficiency can remain as high as 95% at 90 V_{rms} from 20% to 100% of the load.

We can also refer to AND8355 for more general information regarding interleaved PFC stages. This paper particularly focuses on the main characteristics and merits of such a solution.

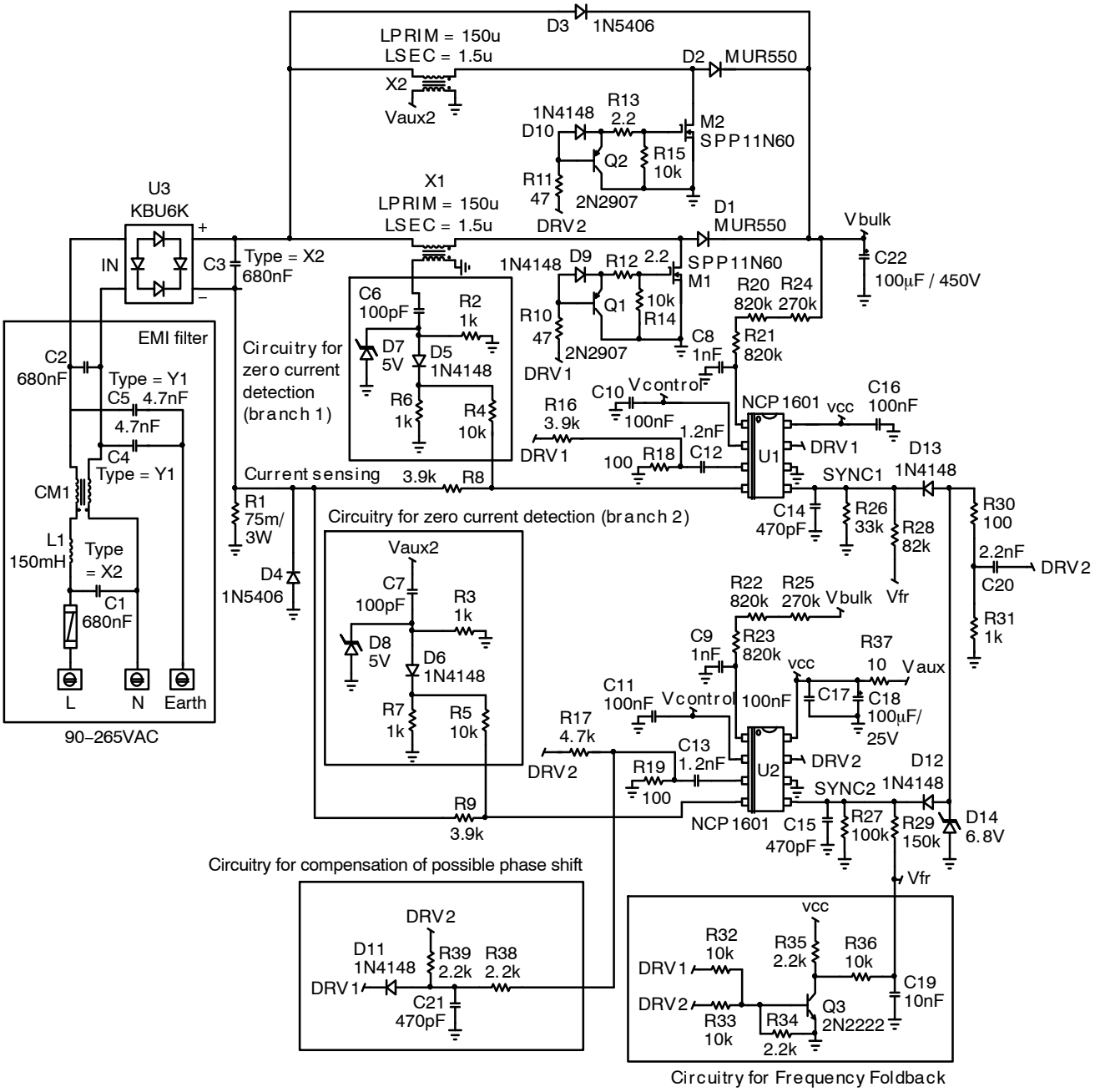

Figure 13. Application Schematic

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81–3–5773–3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative